REMARKS/ARGUMENTS

Applicants have received the Office Action dated March 21, 2006, in which the Examiner: 1) objected to claim 7 because of informalities; 2) rejected claims 1-3, 5, 8-11, 14, 17 and 19 under 35 U.S.C. § 102(b) as being anticipated by Walker et al. (U.S. Pub. No. 2001/0029592, hereinafter "Walker"); 3) rejected claim 18 under 35 U.S.C. § 103(a) as obvious over Walker in view of Erickson et al. (U.S. Pat. No. 6,408,343, hereinafter "Erickson"); 4) rejected claims 4 and 12 as obvious over Walker in view of McKenzie (U.S. Pat. No. 6,453,398, hereinafter "McKenzie"); 5) rejected claims 6 and 13 as obvious over Walker in view of Piccirillo et al. (U.S. Pub. No. 2002/0053010, hereinafter "Piccirillo"); and 6) rejected claims 7 and 16 as obvious over Walker in view of Nakamura et al. (U.S. Pat. No. 5,706,407, hereinafter "Nakamura"). With this Response, Applicants have amended claim 7 to address the objection to claim 7 and traverse the art rejections of the claims.

Walker teaches a memory subsystem that comprises a mechanism (error correction codes) that enables bit errors to be detected and corrected. The error correction mechanism functions upon performing a read operation. See, for example, page 4, paragraph [0045]. In performing error correction during a read operation, error correction is only performed on data that is read—other areas of memory not being read are not tested for errors and thus "areas of memory may sit idle for extended periods thereby allowing data errors to accumulate undetected." Paragraph [0046].

The Examiner focused on paragraph [0040] of Walker which refers to a "cleansing procedure" that "relies on the normal ECC and error logging mechanisms to validate the health of the memory sub-system 40." The cleansing procedure is further detailed in paragraphs [0047]-[0048]. These paragraphs explain that cleansing logic 70 issues its own read commands that are arbitrated along with normal read and write commands. By issuing read commands, the

cleansing logic 70 essentially forces a read of memory for the purpose of checking for errors, since error checking occurs during reads. This is what paragraph [0040] means it states that the cleansing procedure "relies on the normal ECC and error logging mechanisms." The "normal ECC and error logging mechanisms" are the mechanisms that occur during a normal read of memory. Thus, the error detection mechanism of Walker necessarily functions while the memory modules being tested are fully operational and otherwise being used to perform normal read and write operations.

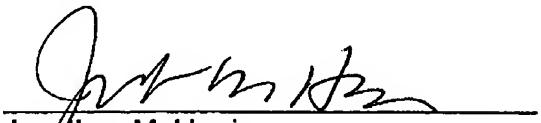
Claim 1 requires, among other limitations, a memory module that "may be isolated wherein transactions that target said isolated memory module can complete without loss of data and without accessing said isolated memory module, and while isolated, said memory module can be tested." Thus, in the context of claim 1, isolating the memory module means not "accessing said isolated memory module," but still being able to complete transactions that target the isolated module. Whereas claim 1 requires testing an isolated memory module, as the term "isolated" is used in claim 1, Walker tests a memory that is not isolated, that is, a memory that continues to be used to perform normal reads and writes. No other art of record satisfies this deficiency of Walker. For at least this reason, claim 1 and all claims dependent thereon are allowable over the cited art.

The remaining independent claims, and their dependent claims, are allowable for the same or similar reasons as claim 1.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including

fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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